This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Currently Amended) A method of operating a data-processing device with an integrated circuit comprising a central processing unit (CPU) and one or more co-processors, in which the integrated circuit performs cryptographic operations, the method comprising: ~~characterized in that~~ in performing ~~a~~ cryptographic operations in the integrated circuit, at least two processors, CPU and co-processors, perform ~~a~~ cryptographic operations simultaneously and in parallel, ~~characterized in that~~ wherein ~~only~~ the cryptographic operations of at least one processor, CPU or co-processor, ~~is a~~ are useful operations and ~~all other~~the cryptographic operations performed by at least one other processor, CPU or co-processor, are dummy operations whose results are rejected, and consumption characteristics of the data-processing device being a superimposition of consumption characteristics associated with performing both useful and rejected cryptographic operations, whereby reconstruction of the consumption characteristics associated with performing any of the useful cryptographic operations is impeded.

3. (Currently Amended) A method as claimed in claim 2, ~~characterized in that~~ wherein the selection as to which processor, CPU or co-processor, performs a useful operation is random-controlled.

4. (Currently Amended) A method as claimed in claim 2, ~~of operating a data processing device with an integrated circuit comprising a central processing unit (CPU) and one or more co-processors, in which the integrated circuit performs cryptographic operations characterized in that in performing a cryptographic operation in the integrated circuit, at least two processors, CPU and co processors, perform a cryptographic operation simultaneously and in parallel, characterized in that~~ wherein a cryptographic operation is

split up into at least two sub-operations and ~~in that~~ at least two processors perform at least one sub-operation in parallel and simultaneously with at least one dummy operation ~~whose results are rejected~~.

5. (Canceled)

6. (Previously Presented) A method as claimed in claim 4, characterized in that the selection as to which processor performs the at least one sub-operation in parallel and simultaneously with at least one dummy operation is random-controlled.

7. (Currently Amended) A method ~~of operating a data processing device with an integrated circuit comprising a central processing unit (CPU) and one or more co-processors, in which the integrated circuit performs cryptographic operations characterized in that in performing a cryptographic operation in the integrated circuit, at least two processors, CPU and co-processors, perform a cryptographic operation simultaneously and in parallel, characterized in that a cryptographic operation is split up into at least two sub-operations, and at least one sub-operation is performed simultaneously and in parallel with at least one dummy operation by the processors, CPU and co-processors, while~~ as claimed in claim 4, wherein subsequently corresponding sub-results from the respective sub-operations are combined ~~and the at least one dummy operation results are rejected~~ to an overall result of the overall cryptographic operation.

8. (Original) A method as claimed in claim 7, characterized in that the split-up of the cryptographic operation into sub-operations is random-controlled.

9. (Previously Presented) A method as claimed in claim 7, characterized in that the sub-operations are parts of an encryption in accordance with Data Encryption Standard (DES).

10. (Currently Amended) A data-processing device with an integrated circuit, comprising: a central processing unit (CPU) and one or more co-processors, ~~characterized in that the integrated circuit comprises~~ a control unit which controls the ~~processors,~~ CPU and co-processors ~~in such a way~~ so that, in the case of a cryptographic operation, at least two ~~processors~~ of the CPU and co-processors perform a cryptographic operation simultaneously and in parallel with at least one dummy operation,~~.~~ whereby consumption characteristics associated with performing the respective cryptographic and dummy operations are superimposed so that reconstruction of the consumption characteristics associated with performing the cryptographic operation is impeded.

11. (Currently Amended) A data-processing device as claimed in claim 10, ~~characterized in that~~wherein the control unit comprises a splitter which splits ~~up a~~ cryptographic operation into at least two sub-operations~~,~~ and at least one of the sub-operations and at least one dummy operation is supplied for simultaneous processing to two separate ~~processors of~~ the ~~integrated circuit,~~ CPU and co-processors.

12. (Currently Amended) A data-processing device as claimed in claim 11, ~~characterized in that~~ wherein the control unit further comprises a recombiner which recombines each sub-result of the sub-operations simultaneously performed by the CPU and co-processors and the at least one dummy operation results are rejected to an overall result of the overall cryptographic operation.

13. (Currently Amended) A data-processing device as claimed in claim 12, ~~with an integrated circuit comprising a central processing unit (CPU) and one or more co-processors, characterized in that the integrated circuit comprises a control unit which controls the processors, CPU and co-processors in such a way that, in the case of a cryptographic operation, at least two processors perform a cryptographic operation simultaneously and in parallel, the control unit comprises a splitter which splits up a~~

~~cryptographic operation into at least two sub operations and supplies them for simultaneous processing to two separate processors of the integrated circuit, CPU and co-processors, the control unit further comprises a recombiner which recombines each sub-result of the sub operations simultaneously performed by the processors , characterized in that~~ wherein the splitter ~~is formed in such a way that~~splits a cryptographic operation so that at least one sub-operation is a dummy operation, and ~~in that~~ wherein the recombiner ~~is formed in such a way that it~~ rejects the relevant result of a processor that has performed ~~a~~such dummy operation.

14. (Currently Amended) A data-processing device ~~of~~ as claimed in claim 13, ~~characterized in that the integrated circuit additionally comprises~~ further comprising a random generator which is connected to the splitter ~~in such a way~~ so that ~~it~~ the splitter operates in a random-controlled manner.

15. (New) A method of performing a cryptographic operation in a data-processing device, the data-processing device including at least two processors, the method comprising: performing a cryptographic operation in a first processor; performing a second operation in a second processor, the second operation being performed simultaneously and in parallel with performing the cryptographic operation so that consumption characteristics of the data-processing device is a superimposition of consumption characteristics associated with performing the cryptographic operation and consumption characteristics associated with performing the second operation; and providing such second operation associated with consumption characteristics complementary to consumption characteristics associated with the cryptographic operation.

16. (New) The method of claim 15, wherein consumption characteristics include current variations associated with performing an operation.

17. (New) The method of claim 15, wherein superimposition of consumption characteristics encrypts temporal fluctuations of current consumption during the cryptographic operation.

18. (New) The method of claim 15, further comprising providing data input relating to the cryptographic operation and providing data input relating to the second operation, the second operation and the data input to the second operation being provided so that performing the second operation using that data input is associated with current variations that are complementary to the current variations associated with performing the cryptographic operation using its data input.

19. (New) The method of claim 18, wherein the cryptographic operation and the second operation are the same, and the data input to the cryptographic operation is a key, and the data input to the second operation is a second key formulated so as to result in said complementary current variation.

20. (New) The method of claim 18, wherein the data input to the cryptographic operation is a key, and the data input to the second operation is the same key, and the second operation is provided so as to result, responsive to the key, in said complementary current variation.

21. (New) The method of claim 15, further comprising splitting a cryptographic operation to form sub-operations, a first such sub-operation being the cryptographic operation and a second such sub-operation being the second operation, such that performing such sub-operations simultaneously and in parallel compensates for asymmetries.

22. (New) The method of claim 15, wherein the second operation comprises a second cryptographic operation, and further comprising using the results from performing the second operation.

23. (New) The method of claim 15, further comprising splitting a cryptographic operation to form the cryptographic operation and the second operation, and further comprising using the results from performing both such operations.

24. (New) The method of claim 15, further comprising rejecting the results from performing the second operation.

25. (New) The method of claim 15, further comprising randomly controlling selection of the processor that performs the cryptographic operation.

26. (New) The method of claim 25, further comprising randomly controlling selection of the processor that performs the second operation.

27. (New) The method of claim 15, further comprising providing superimposition of consumption characteristics such that reconstruction of consumption characteristics associated with the cryptographic operation is impeded in the frequency space.

28. (New) The method of claim 15, wherein consumption characteristics include one or more of power, current, temperature, or other indirect radiation associated with performing an operation.